**ECE -1 Lab **

**Experiment - 1**

**Aim:** Design, simulate and implement Half adder, Full adder using dataflow, behavioral and structural modeling in VHDL.

Description:

Part1:

1. Design and implement half adder using data flow modeling.
2. Design and implement Half adder using Behavioral modeling by using If statement.
3. Implement Full adder using data flow modeling.
4. Implement full adder using Behavioral modeling by using If statement.
5. Implement full adder using structural modeling with the use of half added modules.

Part2:

1. For each type of the above implementations generate the synthesis report.
2. Make one appropriate testbench waveform file for each experiment and verify the testbench.
3. Compare delay and cell usage for 2 half adders and 3 full adders.